IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Case No. 11521US02 **PATENT**

In the Application of:

DANIEL J. MARCHOK et al.

Serial No.: to be assigned

Filed: herewith

For: APPARATUS AND METHOD FOR SYMBOL ALIGNMENT IN A MULTI-POINT OFDM/DMT DIGITAL COMMUNICATIONS SYSTEM

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all correspondence referenced herein are being deposited with the United States Postal Service as express mail in an envelope addressed to the Asst. Commissioner for Patents, United States Patent and Trademark Office, BOX APPLICATION, Washington DC 20231 on July 25, 2001 as No. EL649150611US.

By: Ronald E. Larson
Ronald E. Larson
Reg. No. 24,478

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
BOX APPLICATION
Washington, DC 20231

Dear Sir:

Kindly amend the above-identified application as follows:

In the Specification:

Kindly amend the specification by substituting new paragraphs according to the following instructions. An attachment showing the changes in the paragraphs appears at the end of this Preliminary Amendment.

Page 1, after "CROSS-REFERENCE TO RELATED APPLICATIONS," kindly delete the present paragraph and substitute:

The present application is a continuation-in-part application of U.S.S.N. 08/700,779, filed August 22, 1996 and a continuation of Application No. 08/845,544, filed April 24, 1997.

On page 15, kindly delete the second paragraph and substitute:

It will be recognized that an FFT can be performed on the reduced subset of received bins yet still reap the advantages inherent in the disclosed receiver architecture. This is due to the fact the FFT can be implemented using a digital signal processor of reduced complexity when compared to an FFT processing the entire bandwidth transmitted by the head end unit 25.

On page 16, kindly delete the second paragraph and substitute:

The output from the decoding and formatting section 130 is supplied to the input of one or both of a digital-to-analog section 132 and direct digital section 137. The digital-to-analog section 132 converts the digital information received from the decoding and formatting section 130 to an analog signal that may be supplied to various analog devices. The direct digital section 137 provides an interface between the digital signal output of the decoding and formatting section 130 and any digital data devices.

On page 17, kindly delete the last partial paragraph beginning "The received signal, ..." and on page 18, kindly delete the first paragraph and substitute:

The received signal, now converted to the IF band, is subsequently supplied to the input of an IF bandpass filter 185 that, for example, has a 300 KHz bandwidth and a center frequency of about 10.7 MHz. The output of the bandpass filter 185 is an OFDM/DMT modulated signal having only a subset of the entire number of bins transmitted by the head end unit 25. One or both of the filters 165 and 185, however,

may be used to reduce the bandwidth of the received signal so as to limit the number of bins that are ultimately processed. The filtered IF signal is converted to a digital signal by an A / D converter 190 that has its conversion clock on line 195 synchronized to the reference clock on line 180 through a clock dividing circuit 200. As noted above, the conversion clock frequency may be selected to be low enough to result in undersampling of the IF signal thereby reducing the number of samples supplied at the A/D converter 190 output. An increase in the sampling rate, however, can be used to compensate for any inexactness of filters 165 and/or 185.

On page 18, kindly delete the last partial paragraph beginning "FIG. 8 illustrates ..." and on page 19, kindly delete the first paragraph and substitute:

FIG. 8 illustrates one embodiment of a hardware correlator 210 that may be used in the Fourier Transform section 125. The illustrated hardware correlator 210 is designed to correlate nine frequency bins within the total bandwidth of frequency bins that are provided in digital format at the output of the A/D converter 190 of, for example, the IF-to-digital circuit 120. The correlator 210 includes a multiplier section 215, a frequency generator section 220, and an accumulator section 225. As shown, the multiplier section 215 receives the digital data that is output from the IF-to-digital section 125 and multiplies each value by the sine and cosine value of each of the nine frequency bins. The sine and cosine values are supplied as inputs to the multiplier 215 from the frequency generator section 220. The frequency generator section 220 includes a step-size register 227 that includes, in the present embodiment, nine register locations that are programmed by a microcontroller or digital signal processor. The values stored in the step-size register 227 are used to determine the step-size of the

addresses supplied to address the data in a cosine table ROM 230, shown here as a quarter wave cosine table. An address modifier circuit 235 receives the address data from the address register 240 and modifies the data so that the address data supplied to the cosine table ROM 230 falls within an acceptable range of addresses and thereby accesses the proper portion of the wave. A sine/cosine bit is supplied from, for example, the timing and control circuit 140 so that each value received from the IF-to-digital converter 125 is multiplied by both the sine and cosine values of each of the nine frequency bins. The data resulting from the multiplication operation are accumulated in the accumulator section 225 and output to the decoder/formatting section 130 for further processing.

On page 21, kindly delete the second paragraph and substitute:

The serial data stream output from the data interface unit 315 is supplied to the input of the transmit engine circuit 320. The data that the transmit engine circuit 320 receives includes one constellation point for each OFDM/DMT bin of the reduced set of bins that is active during a single symbol time. The transmit engine circuit 320 is responsible for calculating the Inverse Fourier Transform on the data stream that is to be modulated and for producing a time domain sequence for each symbol along with any cyclic prefix. Generally, systems using OFDM/DMT modulation perform this function using an IFFT that is implemented, for example, with a digital signal processor. However, in a multi-point application, such as the communication system disclosed herein, only a limited number of the possible frequencies or bins is used by each secondary transmitter. Given that only a portion of the total available transmission

bandwidth is utilized, the disclosed secondary transmitter architecture is more efficient and cost-effective.

On page 31, kindly delete the last partial paragraph beginning "In operation, ..." and on page 32, kindly delete the first paragraph and substitute:

In operation, given the foregoing assumptions, the sample needed for tap 101 is first latched into register 635. The sample needed for tap 1 is then latched into register 640. The two samples are added to one another by adder 645. The resulting sum is supplied to the input of digital multiplier 650 where it is multiplied by the coefficient for tap 1 as supplied from the coefficient table memory 655. The resulting digital value is effectively stored in register 665 of the accumulator 675 (the initial value contained in register 665 is assumed to be zero). The same basic operation is next performed for the samples needed for taps 2 and 100, but using the coefficient for tap 2 as supplied from the coefficient table memory 655. The digital value resulting from the multiplication with the coefficient for tap 2, however, is added to the digital value result of the previous multiplication that is already stored in register 665 by the accumulator 675. In the exemplary embodiment, this operation is repeated for a total of 50 times. The 51st operation proceeds in a slightly different matter. More particularly, the data corresponding to tape 51 is stored in register 635, while register 640 is loaded with a zero. These values are added to one another by adder 645 and are multiplied by tap coefficient 51 at multiplier 650. The resulting value is added to the digital value that is already present in register 665. The result is again latched into register 665. As such, register 665 contains a filtered output value. This filtered output value is subsequently

stored in the engine output buffer 670 for subsequent supply to the D/A converter of the digital-to-baseband (or IF) circuit 330 through multiplexer 625 and register 630.

On page 36, kindly delete the second paragraph and substitute:

FIGs. 16 – 18 illustrate one manner of initiating communications between a newly added or powered-up remote service unit 30 and the head end unit 25. As shown at step 720, the remote service unit 30 first synchronizes its internal clocks with the head end unit 25. One way in which this may be accomplished can be described with reference to FIG. 2 which shows a pilot tone added by the head end unit 25 to a predetermined bin output that is transmitted to the remote service units 30. The pilot tone is extracted from the received signal by the receiver of the remote service unit 30 and used, for example, as a reference signal for a phase-locked loop circuit 601. The output of the phase-locked loop 601 is provided to the input of a voltage controlled oscillator 605 which generates the reference clock for the remote service unit 30.

On page 43, kindly delete the second paragraph and substitute:

The phase coefficients used above may be generated in a number of manners. In accordance with a first method, the coefficients are generated "on the fly". To this end, a pair of memory locations in the receiver PC_0 and PS_0 are initialized with the values (1,0). Before the receiver is ready to process the 1th (1 = 1, . . ., L) symbol, the same two memory locations are updated according to:

On page 44, kindly delete the last partial paragraph beginning "A preferred implementation ..." and on page 45, kindly delete the first paragraph and substitute:

A preferred implementation of the RAM block 900 is illustrated in FIG. 19. As shown, a pair of 138 x 4 bit, 2-port RAMs 905, 906 receive data from the analog-to-

digital converter 190 and are connected to supply this data to a digital signal processor 910. The read and write operations to and from the RAMs 905 are under the control of a control and address generator circuit 915 and the digital signal processor 910. The data supplied to the digital signal processor 910 is processed in accordance with the operations described above to attain symbol alignment.

On page 46, kindly delete the last partial paragraph beginning "After the newly added remote ..." and on page 47, kindly delete the first paragraph and substitute:

After the newly added remote service unit has been identified by the head end unit 25, the head end unit 25 commands the newly added remote service unit, via the downstream communications channel, to send, for example, a broad band, periodic signal. The bandwidth of the transmitted signal should be sufficiently broad so that the signal does not interfere with the receipt of transmissions from other remote service units 30 by the head end unit 25. One such broad band signal that may be used is an impulse signal of a predetermined amplitude on the upstream communications channel that is transmitted at the symbol rate. Using the same basic method described above in connection with the remote service unit, the head end unit 25 detects the time position of the impulse signal and provides the remote service unit with the information necessary to align its symbol transmissions with the symbol transmissions of the other remote service units. That is, the head end unit 25 directs the transmitter of the newly added remote service unit 30 to transmit its symbols in alignment with symbol transmissions received from other remote service units. After the head end unit 25 has directed the remote service unit 30 to align its symbol transmissions, the remote service unit 30 discontinues further transmission of the broad band periodic signal. Further

communications between the newly added remote service unit and the head end unit 25 can take place on the upstream and downstream communications channels until the head end unit 25 allocates the transmit and receive bins that are to be assigned to the newly added remote service unit and instructs it accordingly. Once the foregoing has been completed, the head end unit 25 and the newly added remote service unit carry out their standard communications at step 760. It should be noted from the foregoing description, that the initialization processes described above take place without interrupting communications between the head end unit 25 and the other remote service units 30 in the system.

On page 47, kindly delete the last partial paragraph beginning "FIGs. 21 and 22 ..." and on page 48, kindly delete the first paragraph and substitute:

FIGs. 21 and 22 illustrate two modifications that may be made to the transmitter illustrated in FIG. 10 to add a predetermined signal, such as the above-mentioned impulse signal, to the upstream data to allow the head end unit 25 to determine where in time the transmitter of the remote service unit 30 is transmitting and direct it to transmit in the appropriate upstream time slot. In the embodiment of FIG. 21, an adder 920 is connected to receive the output of register 925 and the output of a sequence ROM or generator circuit 930. The sequence ROM 930 receives sequence sample selection signals along one or more lines 935 provided by the timing and control circuit 940. In response to these signals, the sequence ROM 930 provides digital data values along one or more lines 945 to the input of the adder 920. These digital data values correspond to the predetermined signal, such as the above-noted impulse signal, that is added to one or more symbols of the upstream data transmission or, alternatively,

transmitted alone without the transmission of upstream symbols. The timing and control circuit 940 provides the appropriate sequence sample selection signals required to add the predetermined signal at a given periodic rate.

On page 48, kindly delete the last partial paragraph beginning "In the embodiment of FIG. 22, ..." and on page 49, kindly delete the first paragraph and substitute:

In the embodiment of FIG. 22, an adder/subtractor 950 is connected to receive the output of register 925 and the output of a multiplexer 855. The multiplexer 955 includes two inputs, one input being set to a zero state and the other input being set to a constant value "k". The multiplexer 955 receives its output selection signal along line 960 provided by the timing and control circuit 940. In response to the output selection signal, the multiplexer 955 provides digital data values corresponding to either the "0" or the constant "k" along one or more lines 965 to the input of the adder/subtractor 950 at the appropriate times in the formatted symbol frame. These digital data values correspond to the above-noted impulse signal of amplitude "k" that is either added to or subtracted from one or more symbols of the upstream data transmission. The determination as to whether the constant "k" is added or subtracted is made withint he timing control circuit 940 that provides a selection signal on line 960 to the multiplexer 955 thereby to assign a polarity to the superimposed signal.

On page 63, kindly delete the first part of the only paragraph beginning "A multi-point communication system ..." and on page 64, kindly delete the remainder of the only paragraph and substitute:

A multi-point communication system that comprises a head end unit disposed at a primary site and a plurality of receivers disposed at remote sites. The head end unit includes a transmitter for transmitting OFDM/DMT symbols over a predetermined number of bins across a transmission medium. The OFDM/DMT symbols are transmitted in periodically occurring formatted symbol frames. The cyclic prefix includes a predetermined periodic signal superimposed thereon. The receivers receive the OFDM/DMT symbols over a subset of the predetermined number of bins from the transmission medium and use the superimposed signals to attain symbol alignment. In accordance with a further aspect of the present invention, the receivers apply a predetermined incremental phase shift to received samples corresponding to the received OFDM/DMT symbols to thereby compensate for phase shifts. The multi-point communications system may include a similar system for aligning symbols transmissions from a remote service unit having a transmitter. Such a system includes a plurality of remote service units each including a transmitter for transmitting OFDM/DMT symbols over a predetermined number of bins across a transmission medium. Each of the plurality of remote service units is operable in a symbol alignment mode in which the transmitter transmits a broad band periodic signal. The head end unit includes a receiver for receiving the OFDM/DMT symbols, including the broad band periodic signal, from the transmission medium. The head end unit uses the time position of the broad band periodic signal to align the symbol transmissions of the remote service units.

In the Drawings:

Kindly enter the enclosed formal drawings for Figures 1-22. Please note that Figures 2, 6, 10 and 19 are based on the corresponding substitute Figures submitted with the Amendment And Response To First Office Action mailed July 8, 1999 in the parent application.

In the Claims:

Kindly cancel claims 1-32 and substitute the following new claims 33-48:

33. A communication system employing radio frequency mixing frequencies to transmit and receive data symbols comprising:

a transmitter of at least one predetermined signal; and

at least one unit responsive to the at least one predetermined signal to adjust the phase of at least some of the received data symbols to compensate for differences in the mixing frequencies and to align at least some of the transmitted data symbols with at least some of the received data symbols.

34. The system of claim 33 wherein the at least one unit is responsive to the at least one predetermined signal to adjust the phase of at least some of the received data symbols by rotating the phase of the at least some received data symbols.

35. The system of claim 33 wherein the at least one predetermined signal comprises a pilot tone.

36. The system of claim 33 wherein the at least one predetermined signal comprises an impulse signal.

37. The system of claim 33 wherein the data symbols comprise one of OFDM and DMT symbols.

38. A method of employing radio frequency mixing frequencies to transmit and receive data symbols comprising:

transmitting at least one predetermined signal;

adjusting the phase of at least some of the received data symbols to compensate for differences in the mixing frequencies in response to the at least one predetermined signal; and

aligning at least some of the transmitted data symbols with at least some of the received data symbols in response to the at least one predetermined signal.

39. The method of claim 38 wherein the adjusting the phase comprises rotating the phase of the at least some received data symbols.

40. The method of claim 38 wherein the at least one predetermined signal comprises a pilot tone.

41. The method of claim 38 wherein the at least one predetermined signal comprises an impulse signal.

42. The method of claim 38 wherein the data symbols comprise one of OFDM and DMT symbols.

43. A communication system arranged to transmit and receive data symbols comprising:

a transmitter of a predetermined signal; and

at least one unit responsive to the predetermined signal to align at least some of the transmitted data symbols with at least some of the received data symbols.

44. The system of claim 43 wherein the predetermined signal comprises an impulse signal.

45. The system of claim 43 wherein the data symbols comprise one of OFDM and DMT symbols.

46. A method of transmitting and receiving data symbols comprising:

transmitting a predetermined signal;

aligning at least some of the transmitted data symbols with at least some of the received data symbols in response to the predetermined signal.

47. The method of claim 46 wherein the predetermined signal comprises an impulse signal.

48. The method of claim 46 wherein the data symbols comprise one of OFDM and DMT symbols.

REMARKS

Most of the amendments to the specification were entered by the Examiner in the parent application in response to the Amendment And Response To First Office Action mailed July 8, 1999.

Date: July 25, 2001

Respectfully submitted,

Ronald E. Larson
Reg. No. 24,478
Attorney for Applicant

McAndrews, Held & Malloy, Ltd.
500 W. Madison, 34th Floor
Chicago, IL 60661
312 775-8000

ATTACHMENT SHOWING AMENDMENTS TO THE SPECIFICATION
Attorney Docket No. 11521US02

Page 1, after "CROSS-REFERENCE TO RELATED APPLICATIONS," kindly delete the present paragraph and substitute:

The present application is a continuation-in-part application of U.S.S.N. 08/700,779, filed August 22, 1996 and a continuation of Application No. 08/845,544, filed April 24, 1997.

On page 15, kindly delete the second paragraph and substitute:

It will be recognized that an FFT can be performed on the [reduce] reduced subset of received bins yet still reap the advantages inherent in the disclosed receiver architecture. This is due to the fact the FFT can be implemented using a digital signal processor of reduced complexity when compared to an FFT processing the entire bandwidth transmitted by the head end unit 25.

On page 16, kindly delete the second paragraph and substitute:

The output from the decoding and formatting section 130 is supplied to the input of one or both of [an analog-to digital section 132] a digital-to-analog section 132 and direct digital section 137. The digital-to-analog section 132 converts the digital information received from the decoding and formatting section 130 to an analog signal that may be supplied to various analog devices. The direct digital section 137 provides an interface between the digital signal output of the decoding and formatting section 130 and any digital data devices.

On page 17, kindly delete the last partial paragraph beginning "The received signal, ..." and on page 18, kindly delete the first paragraph and substitute:

The received signal, now converted to the IF band, is subsequently supplied to the input of an IF bandpass filter 185 that, for example, has a 300 KHz bandwidth and a center frequency of about 10.7 MHz. The output of the bandpass filter 185 is an OFDM/DMT modulated signal having only a subset of the entire number of bins transmitted by the head end unit 25. One or both of the filters 165 and 185, however, may be used to reduce the bandwidth of the received signal so as to limit the number of bins that are ultimately processed. The filtered IF signal is converted to a digital signal by an A / D converter 190 that has its conversion clock on line 195 synchronized to the reference clock on line 180 through a clock dividing circuit 200. As noted above, the conversion clock frequency may be selected to be low enough to result in undersampling of the IF signal thereby reducing the number of samples supplied at the A/D converter 190 output. An [increased] increase in the sampling rate, however, can be used to compensate for any inexactness of filters 165 and/or 185.

On page 18, kindly delete the last partial paragraph beginning "FIG. 8 illustrates ..." and on page 19, kindly delete the first paragraph and substitute:

FIG. 8 illustrates one embodiment of a hardware correlator 210 that may be used in the Fourier Transform section 125. The illustrated hardware correlator 210 is designed to correlate nine frequency bins within the total bandwidth of frequency bins that are provided in digital format at the output of the A/D converter 190 of, for example, the IF-to-digital circuit 120. The correlator 210 includes a multiplier section 215, a frequency generator section 220, and an accumulator section 225. As shown, the multiplier section 215 receives the digital data that is output from the IF-to-digital section 125 and multiplies each value by the sine and cosine value of each of the nine

frequency bins. The sine and cosine values are supplied as inputs to the multiplier 215 from the frequency generator section 220. The frequency generator section 220 includes a step-size register 227 that includes, in the present embodiment, nine register locations that are programmed by a microcontroller or digital signal processor. The values stored in the [step-size register 225] step-size register 227 are used to [determined] determine the step-size of the addresses supplied to address the data in a cosine table ROM 230, shown here [has] as a quarter wave cosine table. An address modifier circuit 235 receives the address data from the address register 240 and modifies the data so that the address data supplied to the cosine table ROM 230 falls within an acceptable range of addresses and thereby accesses the proper portion of the wave. A sine/cosine bit is supplied from, for example, the timing and control circuit 140 so that each value received from the IF-to-digital converter 125 is multiplied by both the sine and cosine values of each of the nine frequency bins. The data resulting from the multiplication operation are accumulated in the accumulator section 225 and output to the decoder/formatting section 130 for further processing.

On page 21, kindly delete the second paragraph and substitute:

The serial data stream output from the data interface unit 315 is supplied to the input of the transmit engine circuit 320. The data that the transmit engine circuit 320 receives includes one constellation point for each OFDM/DMT bin of the reduced set of bins that is active during a single symbol time. The transmit engine circuit 320 is responsible for calculating the Inverse Fourier Transform on the data stream that is to be modulated and for producing a time domain sequence for each symbol along with any cyclic prefix. Generally, systems using OFDM/DMT modulation [performs] perform

this function using an IFFT that is implemented, for example, with a digital signal processor. However, in a multi-point application, such as the communication system disclosed herein, only a limited number of the possible frequencies or bins is used by each secondary transmitter. Given that only a portion of the total available transmission bandwidth is utilized, the disclosed secondary transmitter architecture is more efficient and cost-effective.

On page 31, kindly delete the last partial paragraph beginning "In operation ..." and on page 32, kindly delete the first paragraph and substitute:

In operation, given the foregoing assumptions, the sample needed for tap 101 is first latched into register 635. The sample needed for tap 1 is then latched into register 640. The two samples are added to one another by adder 645. The resulting sum is supplied to the input of digital multiplier 650 where it is multiplied by the coefficient for tap 1 as supplied from the coefficient table memory 655. The resulting digital value is effectively stored in register 665 of the accumulator 675 [(the] (the initial value contained in register 665 is assumed to be zero). The same basic operation is next performed for the samples needed for taps 2 and 100, but using the coefficient for tap 2 as supplied from the coefficient table memory 655. The digital value resulting from the multiplication with the coefficient for tap 2, however, is added to the digital value result of the previous multiplication that is already stored in register 665 by the accumulator 675. In the exemplary embodiment, this operation is repeated for a total of 50 times. The 51st operation proceeds in a slightly different matter. More particularly, the data corresponding to tape 51 is stored in register 635, while register 640 is loaded with a zero. These values are added to one another by adder 645 and are multiplied by tap

coefficient 51 at multiplier 650. The resulting value is added to the digital value that is already present in register 665. The result is again latched into register 665. As such, register 665 contains a filtered output value. This filtered output value is subsequently stored in the engine output buffer 670 for subsequent supply to the D/A converter of the digital-to-baseband (or IF) circuit 330 through multiplexer [62 history5] 625 and register 630.

On page 36, kindly delete the second paragraph and substitute:

FIGs. 16 – 18 illustrate one manner of initiating communications between a newly added or powered-up remote service unit 30 and the head end unit 25. As shown at step 720, the remote service unit 30 first synchronizes its internal clocks with the head end unit 25. One way in which this may be accomplished can be described with reference to FIG. 2 which shows a pilot tone added by the head end unit 25 to a predetermined bin output that is transmitted to the remote service units 30. The pilot tone is extracted from the received signal by the receiver of the remote service unit 30 and used, for example, as a reference signal for a [phase-locked loop 600] phase-locked loop 601. The output of the [phase-locked loop 600] phase-locked loop 601 is provided to the input of a voltage controlled oscillator 605 which generates the reference clock for the remote service unit 30.

On page 43, kindly delete the second paragraph and substitute:

The phase coefficients used above may be generated in a number of manners. In accordance with a first method, the coefficients are generated "on the fly". To this end, a pair of memory locations in the receiver PC_0 and PS_0 are initialized with the

values (1,0). Before the receiver is ready to process the 1th (1 = 1, . . ., L) symbol, the same [to] two memory locations are updated according to:

On page 44, kindly delete the last partial paragraph beginning "A preferred implementation ..." and on page 45, kindly delete the first paragraph and substitute:

A preferred implementation of the RAM block 900 is illustrated in FIG. 19. As shown, a pair of 138 x 4 bit, 2-port [RAMs 905] RAMs 905, 906 receive data from the analog-to-digital converter 190 and are connected to supply this data to a digital signal processor 910. The read and write operations to and from the RAMs 905 are under the control of a control and address generator circuit 915 and the digital signal processor 910. The data supplied to the digital signal processor 910 is processed in accordance with the operations described above to attain symbol alignment.

On page 46, kindly delete the last partial paragraph beginning "After the newly added remote ..." and on page 47, kindly delete the first paragraph and substitute:

After the newly added remote service unit has been identified by the head end unit 25, the head end unit 25 commands the newly added remote service unit, via the downstream communications channel, to send, for example, a broad band, periodic signal. The bandwidth of the transmitted signal should be sufficiently broad so that the signal does not interfere with the receipt of transmissions from other remote service units 30 by the head end unit 25. One such [broad and] broad band signal that may be used is an impulse signal of a predetermined amplitude on the upstream communications channel that is transmitted at the symbol rate. Using the same basic method described above in connection with the remote service unit, the head end unit 25 detects the time position of the impulse signal and provides the remote service unit

with the information necessary to align its symbol transmissions with the symbol transmissions of the other remote service units. That is, the head end unit 25 directs the transmitter of the newly added remote service unit 30 to transmit its symbols in alignment with symbol transmissions received from other remote service units. After the head end unit 25 has directed the remote service unit 30 to align its symbol transmissions, the remote service unit 30 discontinues further transmission of the broad band periodic signal. Further communications between the newly added remote service unit and the head end unit 25 can take place on the upstream and downstream communications channels until the head end unit 25 allocates the transmit and receive bins that are to be assigned to the newly added remote service unit and instructs it accordingly. Once the foregoing has been completed, the head end unit 25 and the newly added remote service unit carry out their standard communications at step 760. It should be noted from the foregoing description, that the initialization processes described above take place without interrupting communications between the head end unit 25 and the other remote service units 30 in the system.

On page 47, kindly delete the last partial paragraph beginning "FIGs. 21 and 22 ..." and on page 48, kindly delete the first paragraph and substitute:

FIGs. 21 and 22 illustrate two modifications that may be made to the transmitter illustrated in FIG. 10 to add a predetermined signal, such as the above-mentioned impulse signal, to the upstream data to allow the head end unit 25 to determine where in time the transmitter of the remote service unit 30 is transmitting and direct it to transmit in the appropriate upstream time slot. In the embodiment of [FIG. 20] FIG. 21, an adder 920 is connected to receive the output of register 925 and the output of a

sequence ROM or generator circuit 930. The sequence ROM 930 receives sequence sample selection signals along one or more lines 935 provided by the timing and control circuit 940. In response to these signals, the sequence ROM 930 provides digital data values along one or more lines 945 to the input of the adder 920. These digital data values correspond to the predetermined signal, such as the above-noted impulse signal, that is added to one or more symbols of the upstream data transmission or, alternatively, transmitted alone without the transmission of upstream symbols. The timing and control circuit 940 provides the appropriate sequence sample selection signals required to add the predetermined signal at a given periodic rate.

On page 48, kindly delete the last partial paragraph beginning "In the embodiment of FIG. 22, ..." and on page 49, kindly delete the first paragraph and substitute:

In the embodiment of FIG. 22, an adder/subtractor 950 is connected to receive the output of register 925 and the output of a multiplexer 855. The multiplexer 955 includes two inputs, one input being set to a zero state and the other input being [sent] set to a constant value "k". The multiplexer 955 receives its output selection signal along line 960 provided by the timing and control circuit 940. In response to the output selection signal, the multiplexer 955 provides digital data values corresponding to either the "0" or the constant "k" along one or more lines 965 to the input of the adder/subtractor 950 at the appropriate times in the formatted symbol frame. These digital data values correspond to the above-noted impulse signal of amplitude "k" that is either added to or subtracted from one or more symbols of the upstream data transmission. The determination as to whether the constant "k" is added or subtracted

is made withint he timing control circuit 940 that provides a selection signal [on line 970] on line 960 to the multiplexer 955 thereby to assign a polarity to the superimposed signal.

On page 63, kindly delete the first part of the only paragraph beginning "A multi-point communication system ..." and on page 64, kindly delete the remainder of the only paragraph and substitute:

A multi-point communication system [is set forth herein. The communications system] that comprises a head end unit disposed at a primary site and a plurality of receivers disposed at remote sites. The head end unit includes a transmitter for transmitting OFDM/DMT symbols over a predetermined number of bins across a transmission medium. The OFDM/DMT symbols are transmitted in periodically occurring formatted symbol frames. The cyclic prefix includes a predetermined periodic signal superimposed thereon. The receivers receive the OFDM/DMT symbols over a subset of the predetermined number of bins from the transmission medium and use the superimposed signals to attain symbol alignment. [Preferably, the superimposed signal is an impulse signal that varies in polarity throughout the transmission cycle and which is superimposed on one or more symbols occurring during a cyclic prefix of the formatted symbol frames. In accordance with a further aspect of the present invention, the receivers apply a predetermined incremental phase shift to received samples corresponding to the received OFDM/DMT symbols to thereby compensate for phase shifts[resulting from the cyclic prefix]. The multi-point communications system may include a similar system for aligning symbols transmissions from a remote service unit having a transmitter. Such a system includes a plurality of remote service units each

including a transmitter for transmitting OFDM/DMT symbols over a predetermined number of bins across a transmission medium. Each of the plurality of remote service units is operable in a symbol alignment mode in which the transmitter transmits a broad band periodic signal. The head end unit includes a receiver for receiving the OFDM/DMT symbols, including the broad band periodic signal, from the transmission medium. The head end unit uses the time position of the broad band periodic signal to align the symbol transmissions of the remote service units[with other ones of the remote service units].